

Water-Borne Fluorinated Polyimide Dielectric for Large-Area IGZO Transistors and Logic Gates

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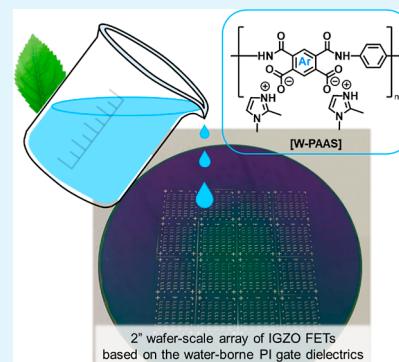
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Supporting Information

ABSTRACT: Thin-film transistors offer excellent and uniform electrical properties over large areas, making them a promising option for various future electronic devices. Polyimide dielectrics are already widely used in various electronic devices because of their exceptional dielectric properties, thermal stability, and desirable mechanical flexibility, which make them suitable for harsh environments. However, the current research on polyimide dielectric materials has certain limitations, such as the use of toxic solvents, high-temperature processes, and deficient coating properties. Herein, we introduce an aromatic polyimide dielectric, which exhibits excellent electrical properties even when processed at a low temperature of 250 °C using environmentally friendly water-based “one-step” polymerization. Despite its thin thickness of <200 nm, the water-borne fluorinated polyimide dielectric material demonstrates stable insulating properties over a wide range of electric fields and achieves a high breakdown voltage of over 4.5 MV cm⁻¹. Furthermore, we successfully achieved a large-area coating of uniform dielectric layers with no pinholes using only water as a solvent and a simple solution process without any additional processing steps. These results demonstrate that the water-borne polyimide gated indium–gallium–zinc oxide transistor exhibits excellent and stable device performance. Moreover, we used the transistor to successfully demonstrate various logic gates (NOT, NAND, and NOR). Overall, this study provides guidelines for the eco-friendly and sustainable use of water-borne polyimide dielectric materials with high electrical performance and large-processing window advantages.

KEYWORDS: polymer gate dielectric, water-borne fluorinated polyimide, large-area coating, IGZO, transistor array



1. INTRODUCTION

Thin-film transistors (TFTs) have been commercialized for flat panel displays because of their high electrical performance and uniform production over large areas.^{1–3} The further development of TFTs holds excellent promise for diverse applications, including electronic skins, foldable displays, energy storage, and bioelectronics.^{4–9} Dielectric materials are crucial to the functionality of these devices, with polymer dielectrics emerging as preferred alternatives to traditional inorganic counterparts because of their remarkable mechanical flexibility and excellent solution processability. Among all polymer dielectrics, polyimide (PI) is widely used in various electronic devices because of its outstanding dielectric properties.^{10–12} Additionally, its exceptional thermal stability, dimensional stability, and chemical resistance further enhance its suitability for use in harsh environments where alternative materials may degrade or fail. Thus, numerous studies have been conducted to utilize PI materials with such advantages as dielectric materials for advanced electronic devices.¹³

However, there are clear limitations in the existing research on PI dielectric materials, including the use of toxic solvents such as *N,N*-dimethylacetamide (DMAc) or *N*-methyl-2-pyrrolidinone (NMP), the high-temperature processes re-

quired for complete imidization, and the resulting significantly reduced coating properties, which may cause pinholes or defects.¹³ Previous research has reported an aromatic PI dielectric film that can be processed with a low temperature of 250 °C through an eco-friendly water-based “one-step” polymerization process.^{14–19} Despite having identical chemical structures in their polymer backbone, water-based PI dielectric films exhibit enhanced hydrolytic stability and consistent formation of pinhole-free thin films in ambient air. Moreover, we have successfully demonstrated a large-area bar-coating process for water/alcohol-based PI dielectric films using eco-friendly cosolvent engineering. However, there are several key limitations in conducting research on PI materials using these eco-friendly processes: (i) the characterization of 3,3',4,4'-biphenyltetracarboxylic dianhydride (BPDA)-based single aromatic PI structures, (ii) the necessity for delicate cosolvent

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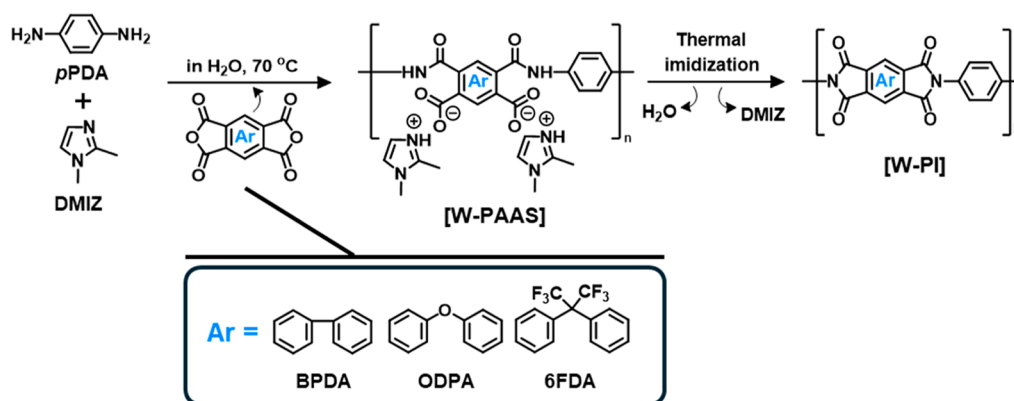


Figure 1. Synthesis scheme of W-PI.

processes for large-area array applications, and (iii) the predominant focus on evaluations for organic semiconductor-based TFTs. These limitations may hinder the broad application of water-based PI dielectric films in high-performance flexible devices.

Herein, we report a novel water-borne fluorinated PI material with enhanced electrical properties and coating characteristics. These properties were achieved by utilizing water as a solvent in the conventional eco-friendly PI precursor synthesis method. The water-borne fluorinated PI was successfully applied as a dielectric film in large-area and high-performance indium–gallium–zinc oxide (IGZO)-based TFT arrays. Our study presents the synthesis of aqueous PI precursors using various dianhydrides, thereby expanding the repertoire of single PI insulating film structures. The water-borne PI dielectric film exhibits notable electrical properties and can be easily and uniformly deposited through a simple solution process, preventing the formation of pinholes regardless of its structure. The water-borne fluorinated PI dielectric film exhibits robust insulating performance across a broad range of electric fields, even at thicknesses below 200 nm, and it attains a high breakdown voltage exceeding 4.5 MV cm^{−1}. Significantly, our approach enables the deposition of large-area, uniform dielectric films up to 6" using only water as a solvent, thus eliminating the necessity for additional processing steps. To evaluate the applicability of our large-scale gate dielectric, we fabricated a top-gated IGZO transistor array on a two-inch wafer using our water-borne fluorinated PI dielectric material. This resulted in all transistors exhibiting uniform and stable performance. To further extend the scope of our research, the transistors were integrated into intricate circuits, namely, NOT, NAND, and NOR logic gates.

2. EXPERIMENTAL SECTION

2.1. Materials. BPDA (>99%), 4,4'-oxidiphthalic anhydride (ODPA; >99%), and 4,4'-(hexafluoroisopropylidene)diphthalic anhydride (6FDA; >99%) were purchased from Changzhou Sunlight Pharmaceutical Co., Ltd. and used after drying in a vacuum oven at high temperatures of 250, 170, and 190 °C, respectively. Furthermore, *p*-phenylenediamine (pPDA; >98%) was purchased from Tokyo Chemical Industry Co., Ltd. and was used overnight after drying in a vacuum oven at 80 °C to eliminate moisture from the material. Additionally, 1,2-dimethylimidazole (DMIZ; 97%) and DMAc (anhydrous, 99.8%) were purchased from Sigma-Aldrich and used as received.

2.2. Synthesis of Water-Borne Poly(Amic Acid) Salts and Organic Solvent-Based Poly(Amic Acid). Water-borne poly(amic acid) salts (W-PAAS) were synthesized using previously reported

methods,^{16,20} and the detailed synthesis procedures are described in Figure 1. In a typical W-PAAS synthesis procedure, 0.025 mol of pPDA, 0.0625 mol of DMIZ, and 144.6 g of H₂O were added to a 250 mL three-necked flask in a N₂ atmosphere. The mixture was stirred at 25 °C for 1 h, after which 0.025 mol of dianhydride (BPDA or ODPA, or 6FDA) was introduced to it. The resulting mixture was then heated to 70 °C and stirred for a specified time, depending on the type of dianhydride used (i.e., 6 h for BPDA and 18 h for ODPA and 6FDA). The resulting products were clear and viscous solutions.

A comparative group was synthesized in the form of an organic solvent-based poly(amic acid) (O-PAA). O-PAA was synthesized using a standard procedure at 25 °C in an inert atmosphere. Initially, pPDA and 124.3 g of DMAc solvent were introduced into a 250 mL three-necked flask. After stirring at room temperature for 1 h, 6FDA was introduced into the flask to initiate the polymerization process. Subsequently, the reaction mixture was cooled to 0 °C and stirred for 6 h, after which it was heated to room temperature. The resulting O-PAA was a transparent and viscous varnish. The prepared solutions were diluted to a specific concentration to achieve the desired coating thickness, which was determined by the viscosity of each solution. The synthesized W-PAAS and O-PAA solutions were designated as W-XX-PAAS and O-XX-PAA (XX represents the dianhydride type, i.e., BPDA [BP], ODPA [OD], or 6FDA [6F]), respectively.

2.3. Large-Area Coating and metal–insulator–metal Device Fabrication. To fabricate the large-area metal–insulator–metal (MIM) device, patterned aluminum electrodes were prepared on a six-inch Si/SiO₂ wafer. A 30 nm-thick aluminum electrode was deposited onto the substrate through a shadow mask (width × length = 1 × 3 mm) via thermal evaporation at a pressure of 1 × 10^{−6} Torr. The Si/SiO₂ substrates were subjected to sonication in isopropyl alcohol for 20 min, followed by O₂ plasma treatment (Harrick Plasma, 18W) for 5 min. The W-PAAS and O-PAA solutions (3–10 wt %) were spin-coated at 2000–3000 rpm for 60–80 s and subsequently preannealed at 80 °C for 30 min under ambient conditions. W-PI was imidized via step-annealing from 100 to 250 °C, with 50 °C increments at 1 h intervals under vacuum. The imidization for O-PI included additional step-annealing from 250 to 350 °C, also with 50 °C increments at 1 h intervals. The synthesized W-PI and O-PI thin films were designated as W-XX-PI or O-XX-PI (XX represents the dianhydride type, i.e., BP, OD, and 6F). The thickness of the gate dielectric films was found to be 149–243 nm using an alpha-step surface profiler.

2.4. Fabrication of the IGZO Transistor Array. Source/drain electrodes were prepared by depositing a 30 nm-thick ITO layer on a Si/SiO₂ wafer through radio frequency magnetron sputtering. Conventional photolithography (AZ 5214E) was used to pattern the ITO layer, where 35 vol % hydrochloric acid diluted in distilled water was used as a wet etchant. To prepare the IGZO precursor solution, indium nitrate hydrate (0.085 M), gallium nitrate hydrate (0.0125 M), and zinc acetate dehydrate (0.0275 M) were dissolved in a 2-methoxyethanol solvent. The precursor solution was then stirred with a magnetic stirrer on a hot plate at 65 °C for 12 h. The solution

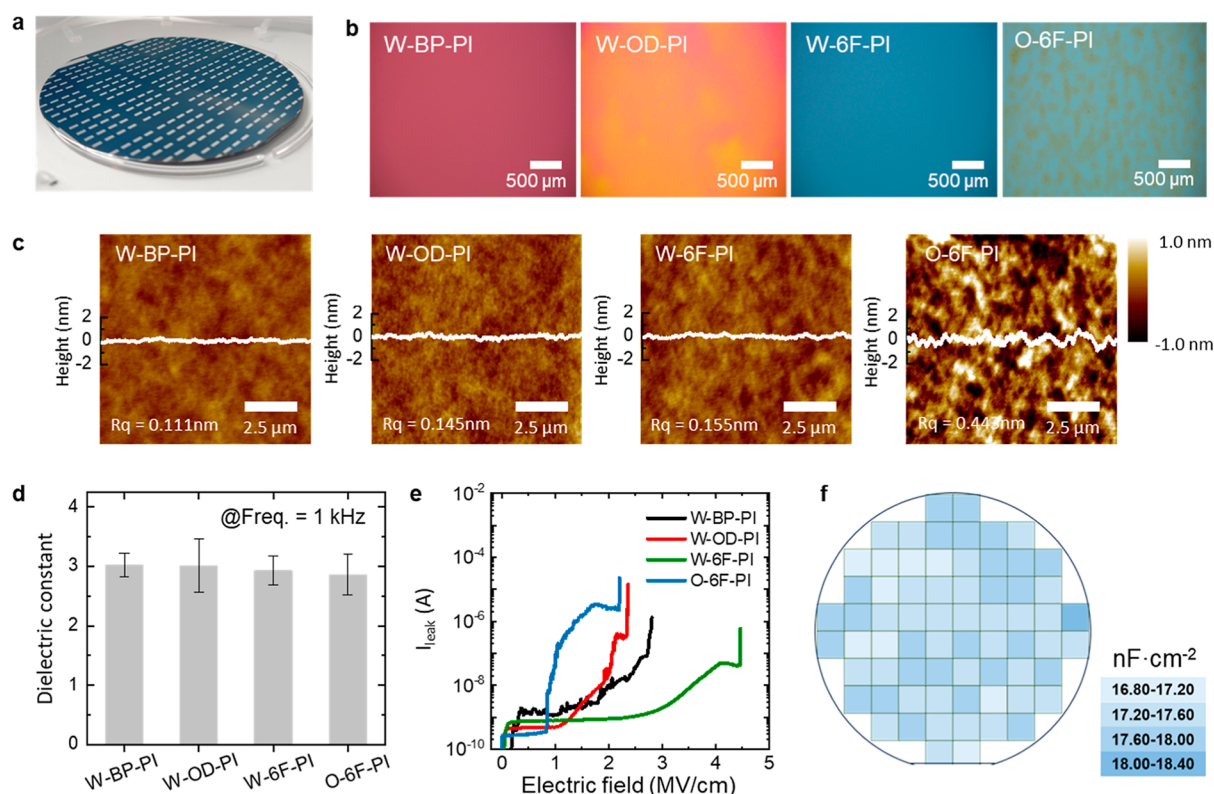


Figure 2. Coating and insulating properties of the W-PI and O-PI dielectric thin films. (a) Spin-coating image of the large-area MIM capacitor on a 6" wafer. (b) Coating properties of W-BP, OD, 6F-PIs, and O-6F-PI. (c) AFM images of the W-PI and O-PI dielectric thin films. (d) Dielectric constants and (e) leakage current–electric field characteristics of the W-PI and O-PI dielectric thin films measured with MIM devices. (f) Areal capacitance distribution chart of the large-area MIM capacitor on 6" wafer.

was spin-coated onto the prepared wafer at 4000 rpm for 30 s and then soft-baked at 60 °C for 120 s on a hot plate. A subsequent annealing process was performed at 450 °C for 300 s. Conventional photolithography (AZ 5214E) was used to define the channel area, and 3 vol % LCE-12 (Cyantek Co.) diluted in distilled water was used as the etchant. The prepared wafers were exposed to UV light in a UV cleaner for 10 s prior to spin coating W-6F-PI. Thereafter, 5 wt % W-6F-PI solutions were spin-coated onto the wafer in three steps: 500 rpm for 5 s, 1500 rpm for 15 s, and 3000 rpm for 60 s. A four-step annealing process was then performed on a hot plate: 80 °C for 5 min, 100 °C for 30 min, 150 °C for 30 min, and 200 °C for 30 min. Finally, 40 nm-thick Al top-gated electrodes were thermally evaporated through a shadow mask.

2.5. Characterization. To confirm the chemical structure, ¹H nuclear magnetic resonance (¹H NMR) spectroscopy was conducted using a Bruker Advance 8500 MHz spectrometer (500 MHz). The chemical shifts were analyzed using dimethyl sulfoxide-*d*₆ as the reference solvent. Fourier-transform infrared (FT-IR) spectra were collected on a Bruker ALPHA^{II} FTIR spectrometer with an attenuated total reflectance diamond probe and recorded in the 400–4000 cm⁻¹ range. The molecular weight was obtained using a size exclusion chromatography instrument comprising a RI-201H detector (Shodex), an SD-500 pump (FUTECS), a CT-6000 column oven (FUTECS), and an S6300 sample injector (FUTECS). The measurement was conducted in an NMP solution with 0.02 M of H₃PO₄ and 0.02 M of LiBr. The columns had three poly(hydroxy methacrylate) columns (multipore) with molar masses ranging from 200 to 20,000,000 g mol⁻¹. The surface morphology of the PI thin films was examined using an optical microscope (Nikon 50-POL). The thickness of the material was determined using an alpha-step surface profiler (KLA-Tencor α-step DC50). The surface morphologies of the PI thin films and pentacene layers at the nanoscale were observed using an atomic force microscope (Bruker Multimode-8) in tapping mode. The surface energy was characterized by measuring the

contact angles of deionized water and diiodomethane on the films using a contact angle analyzer (SEO Phoenix 450). The electrical characteristics of the transistors were evaluated using a Keithley 4200A-SCS semiconductor parameter analyzer. The capacitance and dissipation factor of the MIM capacitors were measured using an Agilent E4980A precision LCR meter within a frequency range of 20 Hz to 100 kHz. All electrical performances were evaluated under ambient conditions. The electrical properties of the transistors and logic gates were measured using a probe station and Keithley 4200A-SCS instrument.

3. RESULTS AND DISCUSSION

The synthetic route for the water-borne PI materials is shown in Figure 1. Three polymers with different dianhydride structures (BPDA, OPA, and 6FDA) were designed and polymerized in a water medium in the presence of DMIZ as an organic base. The O-6FDA-pPDA system was synthesized in DMAc solvent and used as a comparison group. The synthesized W-PAAS and O-PAA were characterized. Specifically, the chemical structure was investigated using ¹H NMR spectroscopy, and the spectrum is depicted in Figure S1. In the W-PAAS series, protons from DMIZ were identified at 2.29, 3.54, 6.79, and 7.03 ppm, and the quaternary proton was unambiguously assigned at 10.5–12.0 ppm owing to salt formation with a carboxylic acid of W-PAAS. The typical aromatic protons were broadly observed at 7.0–8.5 ppm, and no carboxylic acid peaks appeared. Based on the characterization, we confirmed that W-PAAS with different dianhydrides were well synthesized in the aqueous medium. The weight-average molecular weight (M_w) was determined via gel permeation chromatography. The W-PAAS series and O-6F-

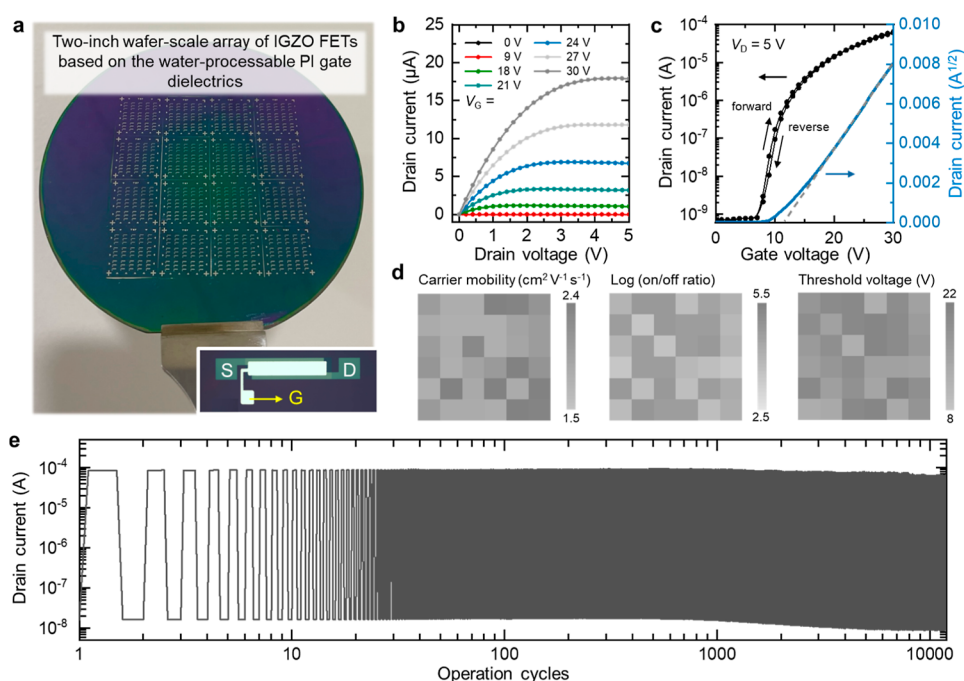


Figure 3. W-6F-PI top-gated IGZO transistor array. (a) Optical image of the W-6F-PI top-gated IGZO transistor fabricated on a two-inch wafer. Inset: optical image of the single transistor device. (b) Output characteristic of the W-6F-PI top-gated IGZO transistor. (c) Transfer characteristic of the W-6F-PI top-gated IGZO transistor. The drain current is shown on the log scale (black), and its root square is displayed on the linear scale (blue). The dotted gray line is the linear fitted line at the maximum transconductance. (d) Color maps of the carrier mobility, on/off current ratio, and threshold voltage distribution of 36 transistor devices. (e) Operational stability test results.

PAA had Mw values of 20,000–26,000 and $\sim 55,000$ g mol⁻¹, respectively (Table S1). To verify if the precursor converted to PI, we analyzed the structural features of the PI using FT-IR spectroscopy (Figure S2a). According to previous reports,^{18,20} the tertiary amine accelerates thermal imidization by forming an active complex with amide groups. W-PAAS with DMIZ can effectively operate as a base catalyst in the imidization reaction, resulting in the completion of imidization at 250 °C. As shown in Figure S2b, the characteristic peaks associated with the N–H stretching of amide and the C=O stretching of amide in W-PAAS were observed at 3500–3000 (broad peak) and 1660 cm⁻¹, respectively. However, after thermal curing up to 250 °C, the main peaks of PI appeared at 1780 (C=O stretching, asym.), 1720 (C=O stretching, sym.), 1380 (C–N stretching), and 740 (imide deformation) cm⁻¹, but there was no peak related to the amide bond of W-PAAS, indicating that W-PAAS was completely converted into W-PI. Conversely, O-6F-PI was completely imidized when the temperature was increased to 350 °C (Figure S2c). These results indicate that the fabrication of a W-PI dielectric using a W-PAAS solution is a more efficient process than the fabrication of an O-PI-based dielectric (Figure S2b).

To confirm the coating ability, surface morphology, and electrical performance of the synthesized water-based and organic-based PI thin films, a MIM device was fabricated on an aluminum electrode-patterned Si/SiO₂ substrate under ambient conditions (Figure 2). The W-PI and O-PI thin films were prepared via spin coating, and the thicknesses of all samples were controlled to ~ 200 nm by adjusting the solution concentration and spin coating speed. Regardless of the solvent or composition, uniform coating characteristics were observed on the 6" substrates (Figure 2a). To analyze the wettability of W-PAAS, we measured the contact angle of W-PAAS (Figure S3). The W-6FDA sample exhibited the lowest contact angle

on Si/SiO₂ substrate, indicating the best coating properties among the samples. The optical microscopy images revealed that the W-PI thin films exhibited uniform surfaces after thermal imidization, albeit with slight variations depending on the composition. Among the samples, W-OD-PI exhibited the least uniform thickness, while W-6F-PI demonstrated enhanced wetting and coating properties, rendering it suitable for large-area substrates. In contrast, the O-6F-PI film prepared using the DMAc solvent displayed notable thickness variations and macroscopic defects (Figure 2b). This observation corroborates previous findings indicating that the thermal imidization process in O-PAA systems markedly influences the surface structure of the thin film because of the removal of water during the heating process.²⁰ To compare the imidization reactions of O-PAA and W-PAA, we analyzed FT-IR and thermogravimetric Analysis (TGA) measurements (Figure S4). According to the TGA results, water generated during the imidization process is removed along with DMIZ (bp = 204 °C) during thermal treatment. The organic base (DMIZ), which participates in the reaction, also functions as a low-temperature curing organic catalyst, enabling the imidization reaction to proceed at a lower temperature compared to O-PAA. More than 90% of the imidization process is completed at 200 °C. Since DMIZ forms a stable salt in water, the W-PI film can maintain its integrity without forming pinholes, even when water is released during the imidization process. The surface morphology of each thin film was examined in detail using atomic force microscopy (AFM; Figure 2c). The water-borne PI films of W-BP, W-OD, W-6F-PI had Rq values of 0.111, 0.145, and 0.155 nm, respectively, indicating that they had a relatively amorphous and smooth surface when compared to the organic-borne PI. Despite having the same composition as W-6F-PI, the O-6F-PI film exhibited a markedly rougher surface morphology with an Rq

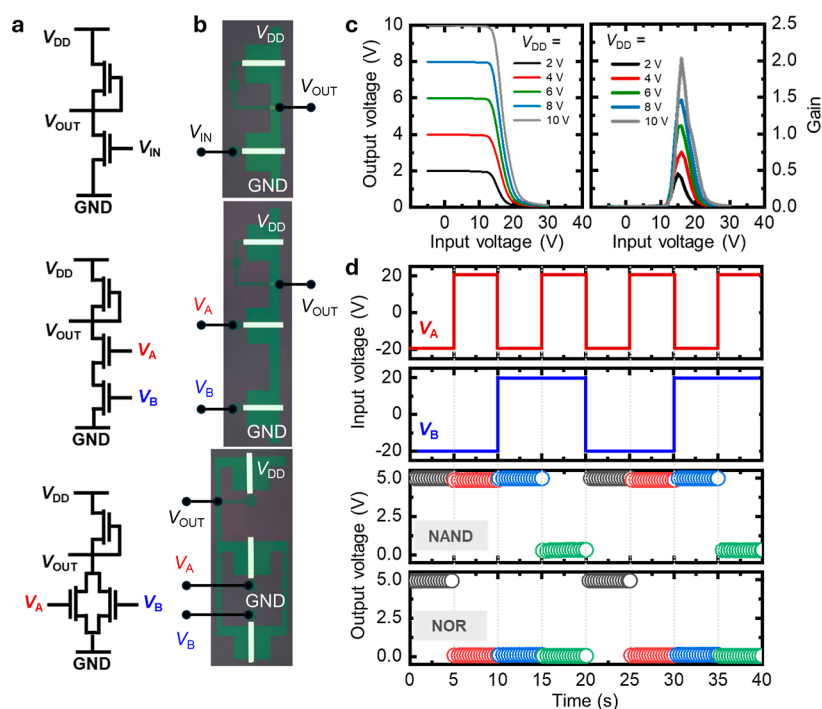


Figure 4. Application in logic circuits. (a) Schematic circuit diagram of the NOT (top), NAND (middle), and NOR (bottom) gates. (b) Optical image of the fabricated NOT (top), NAND (middle), and NOR (bottom) gates. (c) Voltage-transfer characteristic of the NOT gate (left) and the corresponding voltage gain (right). (d) Input voltage signals (top) and the corresponding output voltages for the NAND and NOR gates (bottom).

value of 0.44 nm. This increased surface roughness has the potential to adversely affect device performance.

The dielectric constants of the four W-PI and O-PI thin films were ~ 3 at 1 kHz, which is typical for PI dielectric materials. The introduction of fluorinated moieties slightly reduced the dielectric constant of W-6F-PI to 2.93 (Figure 2d). In contrast, the insulation properties varied significantly with composition and solvent. The leakage current versus electric field characteristics, measured by the MIM devices (Figure 2e), revealed that W-6F-PI had superior insulation properties, with a breakdown voltage of 4.5 MV cm^{-1} , which was significantly higher than those of W-BP-PI and W-OD-PI (below 2.5 MV cm^{-1}). These results demonstrate that W-6F-PI exhibits better insulating properties than other PI-based insulators (Table S2).^{21–29} This suggests the formation of a dense and uniform polymer film, which is a rare achievement for polymer dielectric layers with a thickness of 200 nm. Specifically, because of its excellent coating properties, W-6F-PI exhibited stable insulating characteristics even when coated at a thickness of 150 nm. Consequently, it consistently achieved higher areal capacitance than other dielectric compositions. This high capacitance significantly aids the low-voltage operation of electronic devices. (Figure S5). Despite having the same composition as 6FDA-pPDA, O-6F-PI exhibited a lower breakdown voltage of about 2.2 MV cm^{-1} and the highest leakage current, possibly due to its nonuniform and porous film structure. These results indicate that W-6F-PI has the most favorable coating and insulating properties due to the surface energy differences in the coating solutions. W-6F-PAAS, which had the lowest surface energy (Figure S6), demonstrated excellent wettability on the substrates, resulting in minimal thickness variations and stable electrical properties. Our W-6F-PI dielectric film exhibits superior insulation properties compared to other previously reported dielectrics.

The MIM devices fabricated on these 6" wafers exhibited high areal uniformity in dielectric properties (Figure 2f). Therefore, W-6F-PI was selected as the dielectric layer for subsequent IGZO transistor device studies because of its enhanced electrical stability and coating performance.

A bottom-contact, top-gated IGZO transistor array was fabricated on a two-inch wafer substrate to examine the applicability of W-6F-PI as a large-scale gate dielectric (Figure 3a). In particular, 30 nm-thick ITO electrodes were sputtered and wet-etched through a conventional photolithographic process to form source and drain electrodes. IGZO solutions were spin-coated and patterned to form a semiconducting channel. The channel width and length were defined as 1000 and 100 μm , respectively, for all the measured transistor devices. W-6F-PI solutions were spin-coated on top and sintered to form a gate dielectric layer. Finally, 40 nm-thick Al electrodes were thermally evaporated through a shadow mask to form top-gated electrodes. The inset of Figure 3a shows an optical image of our fabricated bottom-contact, top-gated single transistor device. Figure 3b shows the output characteristic of the transistor. The drain current (I_D) increased with the gate voltage (V_G) and saturated in the high-voltage region, which is the typical behavior of *n*-type transistors. Figure 3c depicts a semilogarithmic plot of a representative transfer characteristic. The black curve (I_D in log-scale) shows that an abrupt current modulation occurred as the V_G was swept in the positive direction, with an on/off current ratio exceeding 5 orders. Negligible hysteresis was detected as the V_G was swept in both forward and reverse directions, which is desirable for reliable transistor operation and logic circuit designs.³⁰ The blue curve represents the square root of I_D in a linear scale, and the dotted gray line is a linear fit at the maximum transconductance, which was used to extract threshold voltage

(V_{TH}) and field-effect mobility (μ).³¹ Eq 1 was used to extract μ from the obtained transfer curves

$$I_{\text{D}} = \frac{C_{\text{S}}\mu(V_{\text{G}} - V_{\text{TH}})^2 W}{2L} \quad (1)$$

where C_{S} is the specific capacitance of the gate dielectric, and W and L are the channel width and length, respectively. Figure S7 shows the transfer characteristics of 36 transistors, and Figure 3d shows spatial mappings of the extracted parameters (μ , V_{TH} , and on/off current ratio). An overall uniform array of transistors was obtained, with $\mu = 2.03 (\pm 0.23) \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, on/off current ratio = $2.8 (\pm 2.2) \times 10^4$, and threshold voltage = $17.48 (\pm 2.73) \text{ V}$. The leakage currents of the 36 devices are also summarized in Figure S8. These parameters were comparable to those of solution-processed IGZO transistors gated with polymer dielectrics (Table S3).^{32–37} Notably, PI materials utilizing the eco-friendly processes were used for the first time as gate dielectrics in solution-processed IGZO transistors. Figure 3e illustrates the operational stability of the W-6F-PI transistor, demonstrating stable performance over 10,000 cycles, in contrast to the W-OD-PI transistor, which exhibited lower tolerance to operation cycles (Figure S9). In addition, the positive bias and temperature stress (PBTs) stability of the device is investigated, as shown in Figure S10. After applying a bias stress for over 2000 s, a positive V_{TH} shift of 5.48 V and negligible change in μ were observed at room temperature (RT). However, at an elevated temperature of 383 K, the V_{TH} shift increased to 8.92 V, accompanied by a degradation in μ of $-0.47 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

The ability to fabricate uniform wafer-scale transistor arrays allowed us to demonstrate more complex circuits. To this end, we applied our transistor devices to NOT, NAND, and NOR logic gates, which are the building blocks for integrated circuits. Figure 4a shows the schematic circuit diagrams of the NOT (top), NAND (middle), and NOR (bottom) gates. Figure 4b shows optical images of the fabricated logic gates. The NOT gate comprises two transistors, with one functioning as the driver transistor and the other as the load transistor. The NAND and NOR gates each utilize three transistors, including one load transistor per gate. Two transistors are connected in series for the NAND gate and in parallel for the NOR gate. Figure 4c illustrates the operation of our NOT gate. The voltage-transfer characteristics under various supply voltages (V_{DD} s) are shown on the left side of Figure 4c. Initially, the output voltage (V_{OUT}) was equal to V_{DD} (logic state “1”) when the input voltage (V_{IN}) was close to 0 V. As V_{IN} was swept to higher voltages, V_{OUT} dropped to 0 V, which corresponds to the logic state “0.” The observed full swing indicates an excellent operation of our NOT gate. The voltage gain ($|dV_{\text{OUT}}/dV_{\text{IN}}|$) of the NOT gate is shown on the right side of Figure 4c; it was above 2 at $V_{\text{DD}} = 10 \text{ V}$. Figure 4d illustrates the operation of both the NAND and NOR gates. The two inputs for each gate are denoted as V_{A} and V_{B} . The low input was set at -20 V (input state “0”) and the high at $+20 \text{ V}$ (input state “1”). All possible input combinations (0,0), (1,0), (0,1), and (1,1) were sequentially applied and repeated for reliability (shown at the top of Figure 4d). The NAND gate outputs a low voltage only when both inputs (V_{A} and V_{B}) are at high voltage levels, while the NOR gate outputs a low voltage when either of the inputs is at a high voltage level. The expected outputs of both NAND and NOR gates for all input combinations are depicted in the bottom part of Figure 4d,

confirming the accurate operation of both logic gates. We also evaluated devices incorporating organic semiconductors to assess their potential for use in future flexible electronic applications (Figures S11, S12, Table S4 and Note S1). Devices using W-6F-PI showed stable operation with high on/off ratios and enhanced mobility, attributed to reduced electron trapping and improved semiconductor alignment on the dielectric surface. These results highlight W-6F-PI's suitability for stable, high-performance flexible electronics.

4. CONCLUSIONS

In conclusion, this paper presents the successful development of an eco-friendly and high-performance fluorinated PI dielectric material, W-6F-PI, specifically designed for large-area IGZO transistor arrays. The enhanced electrical properties and coating characteristics of W-6F-PI were achieved using a water-based “one-step” synthesis method. It is noteworthy that the dielectric material exhibited stable insulation performance even at a reduced thickness of 200 nm, achieving a high breakdown voltage of 4.5 MV cm^{-1} . The scalability and practical application potential of the W-6F-PI dielectric film are demonstrated by its ability to be uniformly deposited over a 6” wafer using a simple, environmentally friendly solution process. The successful fabrication and performance evaluation of large-area IGZO transistor arrays and various logic gates (NOT, NAND, and NOR) revealed uniform and stable device characteristics. This research not only advances our understanding of eco-friendly PI dielectrics but also provides a valuable framework for future innovations in sustainable high-performance electronic devices. Moreover, the environmental sustainability and exceptional electrical performance of W-6F-PI render it a promising candidate for next-generation electronics.

■ ASSOCIATED CONTENT

SI Supporting Information


The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsami.4c14938>.

Additional synthetic scheme, ^1H NMR/FT-IR spectra, SEC trace, TGA thermogram, contact angle/surface energy data, OM/visual image, areal capacitance data, transfer curve, leakage current data, operation stability, and organic semiconductor TFTs data are included in the Supporting Information (PDF)

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Author Contributions

[†]D.K. and Y.A.K. contributed equally. The manuscript was written with the contributions of all authors. All authors have approved the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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